Serial No.: 10/085,903

REMARKS

Claims 1-4, 7-9, 11 and 21-27 stand rejected. Claims 5, 6, 10, 12 and 13 stand objected to as being dependent upon a rejected base claim. Claims 14-20 and 28-33 have been allowed. Appreciation is expressed at this point for the allowance of claims 14-20 and 28-33. Reconsideration of the rejection of claims 1-4, 7-9, 11 and 21-27 is respectfully requested. The Examiner's bases for rejecting those claims are addressed below.

Rejections Under 35 U.S.C. 103(a)

The Examiner rejected claims 1-4, 7-9, 11 and 21-27 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,423,993 to Suzuki et al. in view of U.S. Patent No. 6,380,037 to Osanai. The Examiner's position regarding the alleged combined teachings of Suzuki et al. and Osanai are set forth in paragraph 2 of the instant Office Action. The Examiner has taken the position that the formation of a p+ impurity plug region 39 immediately adjacent to an end of a field oxide region 34[1] constitutes the forming of a dislocation region that traverses the junction of the impurity region 73.

Although the Examiner has focused on the embodiment disclosed in FIG. 11 of Suzuki et al., it may be more useful for the present discussion to focus on FIGS. 8 and 9E. For the convenience of the Examiner, a slightly modified rendition[2] FIG. 8 of the Suzuki et al. patent[3] is enclosed herewith. FIG. 8 shows a cross-sectional view of n-type impurity regions 36 and 33 formed in a substrate that utilizes the field oxide 34 as device isolation. A shallow p+ region 38, the p+ plug 39 and a p-well 352 are formed in the substrate. The Suzuki et al. patentees identified various pn junctions defined by the various impurity regions 33 and 36, the p+ plug 39 and the p-well 352 as follows:

> [i]n addition, in FIG. 8, a high-concentration p-type semiconductor region 38 is formed on the surface of the n-type semiconductor region 36 so as to partially touch

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[1]The field oxide region 34 is variously identified also as a local oxidation of silicon or LOCOS.

[2]Small circles and a series of asterisks have been added to FIG. 8 in order to call out a particular pn junction and the edge of the field oxide region 34.

[3]The element numbering used in Suzuki et al. is followed herein.

> the p-type plug region 39. In the sensor 114, pn-junctions j are formed among each n-type semiconductor region 36 or 33, the p-type semiconductor region 38, the second p-type semiconductor well region 352, and the p-type plug region 39.

Suzuki et al., col. 10, ll. 26-34.

The pn junction between the p+ plug 39 and the impurity regions 36 and 33 is identified by the small circles which trace the pn junction. It is clear from the specification of the Suzuki et al. reference, that the Suzuki et al. patentees were concerned with the potential for leakage currents occurring in the vicinity of the edge of the field oxide region 34. For the convenience of the Examiner, that edge is identified by a series of asterisks in the enclosed FIG. 8 of Suzuki et al. In particular, the patentees were concerned about the possibility for leakage current as a result of dislocations or other crystalline defects at the edge of the field oxide region 34 that might be in close proximity to the various pn junctions. In order to isolate the various pn junctions from the contemplated crystalline defects at the edge of the field oxide region 34, the Suzuki et al. patentees use a separate ion implantation step to form the p+ plug 39.

It is quite clear that the function of the p+ plug 39 is to isolate the end of the field oxide region 34 from the pn junctions defined by the various borders of the impurity regions 36 and 33 as shown in FIG. 8. The applicants described, in conjunction with FIG. 9E, the function of the p+ plug 39 as follows:

> by forming the p-type plug region . . . 39 between the end of the device isolation layer 34 . . . and the n-type semiconductor region 36 . . ., pn-junctions of the photodiode forming the sensor 114 can be isolated from the end of the device isolation layer 34 which has crystal defects such as dislocation . . ., whereby, when the pn-junctions are reverse biased, the depletion layer can be generated at a position apart from the device isolation layer 34.

Suzuki et al., col. 11, ll. 31-40.[4]

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[4]In the quoted passage, selected words have been omitted from the original text in order to improve the readability of the passage. The grammatical construction of the original text does not lend itself to easy reading. This may be due to Japanese grammatical structures that do not easily translate into English.

Applicants respectfully submit that the p+ plug 39 in Suzuki et al. is not a "dislocation region" as that term is used in Applicants' claims. An exemplary definition of "dislocation region" is set forth on page 7, ll. 3-10 of Applicants' specification. The p+ plug region 39 in Suzuki et al. serves a wholly different, indeed utterly opposite function to that of the dislocation region in Applicants' claims. The purpose of the p+ plug 39 in Suzuki et al. is to isolate and thus prevent the flow of charge whereas the dislocation region(s) in Applicants' claims is designed to enable the flow of charge.

Even assuming arguendo that the p+ plug could somehow be deemed to be a dislocation region as used in Applicants' claims, there is remains substantial doubt about whether or not there is any motivation to combine the teachings of Suzuki et al. and Osanai to thereby obtain the claimed invention. Neither reference expresses any concern over the build-up of charge within the body of a device region on a semiconductor-on-insulator substrate. Osanai does disclose a transistor fabrication process using a semiconductor-on-insulator substrate. However there is no discussion therein about the alleviation of charge build-up within the device region above the insulator substrate layer 102.[5] As noted above, Suzuki et al. is concerned with the opposite problem, that is, how to stop the flow of charge from the vicinity of the pn junctions of the photo diode sensor 114.

Conclusion

For the extensive reasons advanced above, Applicants submit that claims 1-13 and 21-27 are patentable and respectfully request that a Notice of Allowability for claims 1-33 issue in due course.

Interview Summary

On June 18, 2003, the undersigned interviewed the Examiner regarding the substance of the instant Office Action. During the interview, the undersigned and the Examiner discussed claim 1 and the teachings of Suzuki et al. The undersigned argued that the p+ plug region 39 identified by the Examiner in the Office Action was not a dislocation region as that term is used in Applicants' claims. Agreement was not reached.

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[5]The element numbering from Osanai is followed herein.

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Miscellaneous

The Assistant Commissioner is authorized to charge any required fees or credit any overpayment to Deposit Account No. 01-0365, Order No. AMDI:115\HON.

Respectfully submitted,

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